AD-A031 207 AIR FORCE AVIONICS LAB WRIGHT-PATTERSON AFB OHIO F/G 17/2
A BIT TIMING EXTRACTION TECHNIQUE.(U)
JUN 76 J J FOSHEE
UNCLASSIFIED AFAL-TR-76-149 NL

1 OF 1
AD A031207

END
DATE FILMED
11-76

AFAL-TR-76-149

12

# A BIT-TIMING EXTRACTION TECHNIQUE

*SYSTEM DEVELOPMENT BRANCH*
*SYSTEM AVIONICS DIVISION*

JUNE 1976






TECHNICAL REPORT AFAL-TR-76-149
FINAL REPORT FOR PERIOD AUGUST 1975 - FEBRUARY 1976



AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

*NOTICE*

*When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.*

This report has been reviewed by the Office of Information and is releasable to the National Technical Information Service (NTIS). At NTIS it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication.

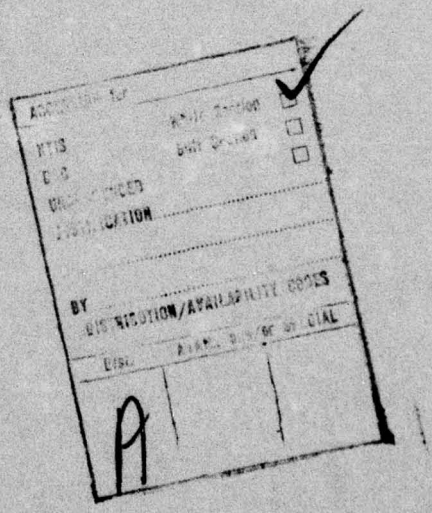
James J. Foshee

JAMES J. FOSHEE
Project Engineer

FOR THE COMMANDER

James D. Everett

JAMES D. EVERETT, Lt Col, USAF
Chief, System Avionics Division
Air Force Avionics Laboratory




***Copies of this report should not be returned unless return is required by security considerations, contractual obligations, or notice on a specific document.***

AIR FORCE - 28 SEPTEMBER 76 - 50

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

## REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

| | |
|---|---|
| 1. REPORT NUMBER: AFAL-TR-76-149 | 2. GOVT ACCESSION NO. |
| 3. RECIPIENT'S CATALOG NUMBER | |
| 4. TITLE *(and Subtitle)*: A Bit Timing Extraction Technique, | 5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report, August 1975 – February 1976 |
| | 6. PERFORMING ORG. REPORT NUMBER |
| 7. AUTHOR(s): James J. Foshee | 8. CONTRACT OR GRANT NUMBER(s) |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS: System Development Branch (AAD), Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio 45433 | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: [redacted] 1227, Task No. 32-08 |
| 11. CONTROLLING OFFICE NAME AND ADDRESS: System Avionics Division (AA), Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio 45433 | 12. REPORT DATE: June 1976 |
| | 13. NUMBER OF PAGES: 65 |
| 14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)* | 15. SECURITY CLASS. *(of this report)*: UNCLASSIFIED |
| | 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE |

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Satellite Communications
Ionospheric Scintillation
Frequency Diversity
Space Diversity
Error-Correction Coding
Bit-Timing Extraction
Acquisition
Data Interleaving
Phase-Lock Loop

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This technical report contains a description of a bit-timing extraction technique which can be used to derive bit-timing (a clock) from a UHF satellite digital communications channel disturbed by the effects of ionospheric scintillation. The bit-timing extraction technique is described as a part of a modulator/demodulator which uses a binary FSK modulator and a post-detection demodulator. In addition a convolutional encoder with a feedback decoder are an integral part of the modulator/demodulator. The functioning of the encoder-decoder requires an accurate clock even during signal fading periods of up to five seconds. The bit-timing extraction technique was conceived to fulfill this need.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

011670

# FOREWORD

This technical report was prepared by personnel of the System Avionics Division (AA), of the Air Force Avionics Laboratory (AFAL), Wright-Patterson Air Force Base, Ohio. This development effort was accomplished during the period of August 1975 through February 1976 under Project No. 1227, "Advanced Microwave Communications," Task No. 3208, "Fade-Resistant Modem."

The Bit-Timing Extractor described in this technical report was conceived and built to operate as a necessary part of the Fade-Resistant Modem. The use of the Bit-Timing Extractor is not necessarily limited to use as a part of the Fade-Resistant Modem. The Bit-Timing Extractor could be used to extract bit-timing in other similar types of digital communications systems.

James J. Foshee was the Project Engineer for this development effort and was responsible for the design of the Fade-Resistant Modem. Francis Ferrara of Technology Scientific Services and Patricia McDaniel of AFAL were also actively involved in the Fade-Resistant Modem program.

TABLE OF CONTENTS

# LIST OF ILLUSTRATIONS

# SECTION I

# INTRODUCTION

With the advent of the ultrahigh frequency (UHF) transponder space satellite (the satellite) the usable range of UHF communications has been extended to basically hemispherical coverage of the earth's surface. By incorporating the satellite into the communications system, mobile terminals, such as an aircraft, can now maintain UHF communications with ground terminals and other mobile terminals as long as each of the terminals is within line-of-sight of the satellite.

Although the satellite extends the coverage of UHF communications, the uplink signal to the satellite and the downlink signal from the satellite must go through the ionosphere. Because of a phenomenon which occurs in the ionosphere, known as ionospheric scintillation, UHF signals passing through the ionosphere can undergo deep fades when this phenomenon is present.

Aarons (Reference 1) has developed models of signal fading caused by the phenomenon of ionospheric scintillation. This phenomenon is a function of the time of year, time of day, location on the earth's surface and a host of other factors and, although this phenomenon does not occur continuously, when it does occur the fading caused by ionospheric scintillation can yield a UHF satellite communications link totally inoperative.

Frequency diversity and space diversity are generally inadequate for use in a UHF satellite communications system disturbed by the effects of ionospheric scintillation. An alternate approach would be to utilize error-correction coding. This approach would not rely on a continuously reliable received signal level but would rely on the error-correction coding to improve system performance. In general, error-correction techniques require reliable bit-timing even during the signal fading periods. The bit-timing extractor would have to extract bit-timing when the receive signal level was adequate and maintain this timing during the signal fades.

# SECTION II

## A FADE-RESISTANT MODEM

An integral part of a UHF satellite digital communications system is the modulator/demodulator (modem) section. There are a number of basic performance requirements for a modem operating as a part of a UHF satellite communications system where ionospheric scintillation fading is a consideration in system design. In general, the modem should have a rapid signal acquisition time without a substantial tradeoff in bit-error-rate (BER) performance. BER is the ratio of the number of bit errors to the total number of bits received during a given time segment. This rapid acquisition time is necessary because the received signal level from the satellite will be intermittently dropping below threshold due to the effects of ionospheric scintillation and the system will be constantly reacquiring the signal. Second, the modem should have the power to correct "burst" errors caused by fading. This is required because of the duration of the fades caused by ionospheric scintillation. Consequently, digital errors often occur in bursts. Third, the modem should be capable of deriving a stable clock which can be adequately maintained during signal fades. This requirement is due to a scheme normally utilized in error-correction codes where the ordinal location of a bit in a digital sequence is important to the error correction process. Therefore, the digital bits must be accurately counted even though some of the bits may be in error due to a signal fade.

Figure 1 contains a block diagram of a modem which meets the basic performance requirements described above. This modem might be called a Fade-Resistant Modem (References 2 and 3) since it would ideally resist the effects of fading. The modem contains a simple binary frequency-shift keyed (FSK) modulator with a dual-filter post-detection demodulator (Reference 4). The modulation technique is similar to, and compatible with, the modulation scheme used in the Air Force Satellite Communications System (AFSCS) (Reference 5). The modulator consists of two stable crystal oscillators separated in frequency by 2500 Hertz (Hz), with one oscillator frequency 1250 Hz above 70 Megahertz (MHz) and the other oscillator 1250 Hz below 70 MHz, and a solid state switch. The digital sequence controls the solid state switch with the lower frequency oscillator representing one binary state (mark) and the higher frequency oscillator representing the other binary state (space). The output of the solid state switch feeds the associated system up/converter. Figure 2 is a block diagram of the FSK modulator. A block diagram of the FSK demodulator is shown in Figure 3. The associated system down/converter feeds the FSK demodulator. In the demodulator the signal is amplified and converted to the 10.7 MHz frequency spectrum. The 10.7 MHz signal is fed through a 5 kilohertz (kHz) bandwidth channel filter and through an amplifier-limiter. The output of the limiter is split, with one output fed to the mark channel and the other output fed to the space channel. Each channel has a 2 kHz bandwidth filter with the center of the

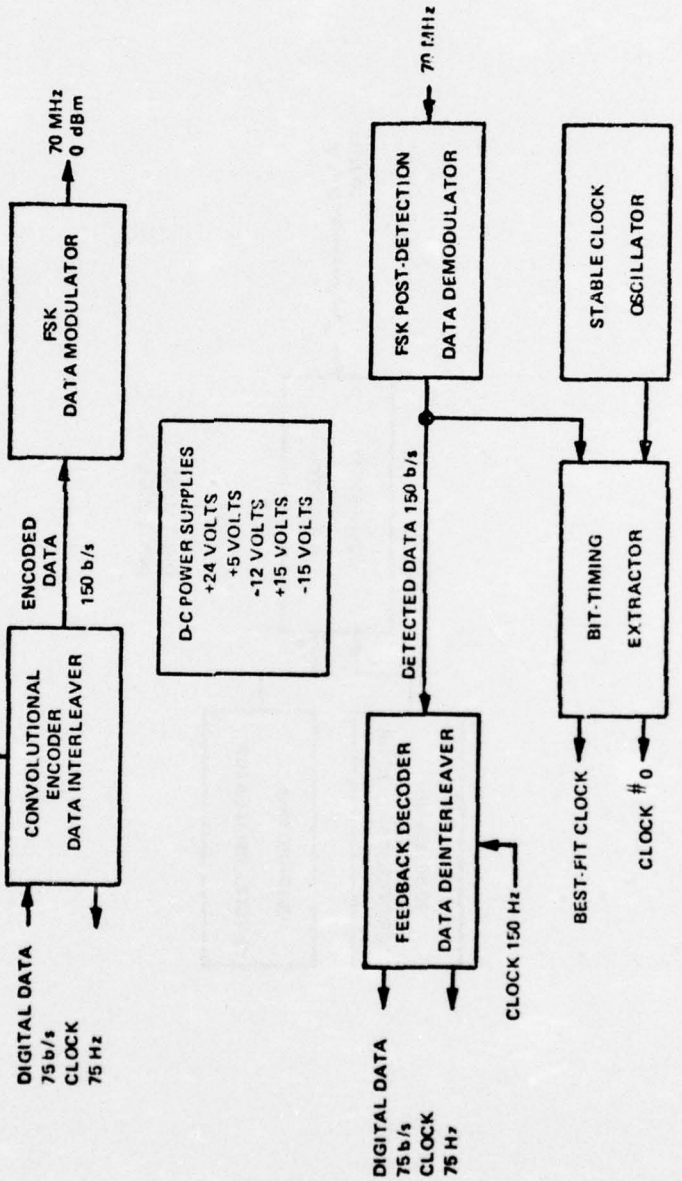



Figure 1. Block Diagram of the Fade-Resistant Modem

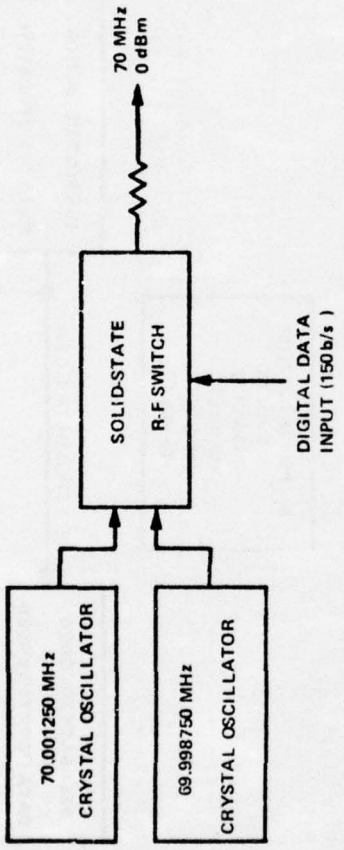



Figure 2. Block Diagram of the FSK Modulator

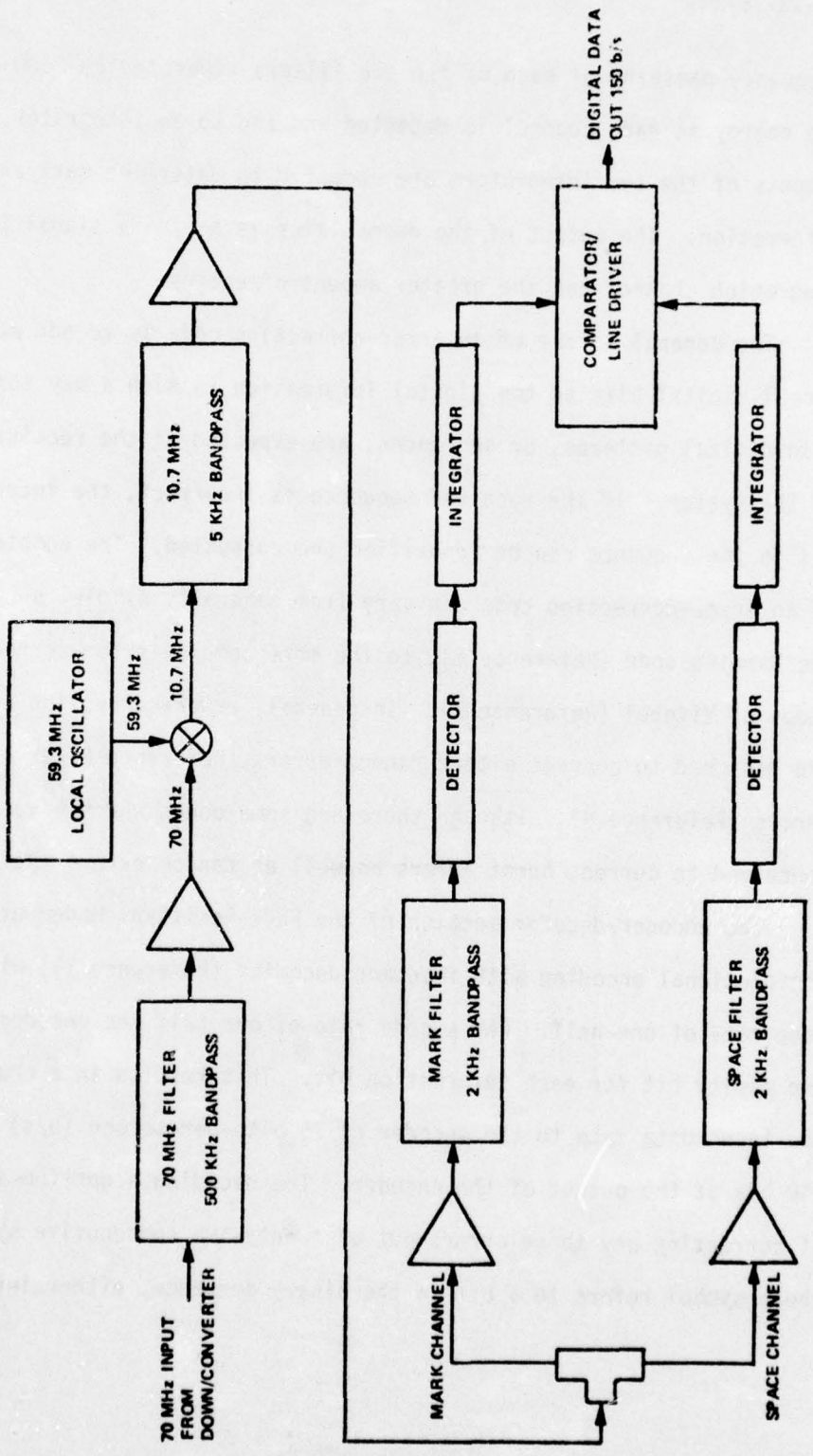



Figure 3. Block Diagram of the FSK Demodulator

frequency passband of each of the two filters separated by 2500 Hz. The energy in each channel is detected and fed to an integrator. The outputs of the two integrators are compared to determine mark and space information. The output of the demodulator is a binary signal indicating which channel has the greater amount of energy.

The general scheme of an error-correction code is to add additional digital bits to the digital information in such a way that certain digital patterns, or sequences, are expected at the receiving end of the system. If the received sequence is incorrect, the incorrect bit in the sequence can be identified and corrected. The complexity of an error-correction code can vary from generally simple, such as the Hamming code (Reference 6), to the more complex error-correction codes of Viterbi (Reference 7). In general, error-correction codes are designed to correct either random errors (Reference 8) or burst errors (Reference 9), although there are some codes which have been conceived to correct burst errors as well as random errors (Reference 10).

The encoder-decoder section of the Fade-Resistant Modem utilizes convolutional encoding with feedback decoding (Reference 11) with a code rate of one-half. For a code rate of one-half the encoder adds one parity bit for each information bit. This results in a change in the input data rate to the encoder of 75 bits-per-second (b/s) to 150 b/s at the output of the encoder. The decoding algorithm is capable of correcting any three errors out of twenty-two consecutive symbols, where symbol refers to a bit in the binary sequence, either information

or parity. The approximate BER performance of the encoder-decoder is given by the following expression (Reference 12):

$$P_{out} \approx 2000\ P_{in}^4$$

where $P_{in}$ is the channel BER at the decoder input and $P_{out}$ is the decoder output BER. This expression is a good approximation of BER performance as long as $P_{in}$ does not exceed .05.

Because the Fade-Resistant Modem is designed to operate with "burst" errors, data interleaving is used to spread adjacent symbols after the data has been encoded. Then at the receiver end of the system, and before the symbols are decoded, the deinterleaving of the symbols tend to spread the errors that may have occurred in bursts and the power of the decoding algorithm can be utilized to correct the errors.

If the separation of adjacent symbols at the output of the interleaver is 256 (this separation is called the interleaving depth), the system could withstand a fade in signal strength of up to 5.12 seconds and yet correct all the errors caused by the signal fade. Since adjacent symbols are separated in time by approximately 1.71 seconds (256 times 1/150) and at least three symbols must be in error, the fade in signal strength must last more than 5.12 seconds to affect three symbols. Since the time required for a twenty-two consecutive symbol block to be transmitted is approximately 37.5 seconds (22 times 1/150 times 256), if another signal fade occurs, in addition to a 5.12 second fade, during a 37.5 second time interval, the decoder may not be capable

of correcting all the errors that were caused by the combination of the signal fades. In general, the combination of encoding and interleaving gives the system the power to withstand various combinations of signal fades over a 37.5 second time interval of up to 5 seconds and yet pass essentially error-free data.

There are basically two problems, among other considerations, associated with the error-correction scheme described above. First of all, the interleaving of the encoded symbols causes a time delay in data transfer. Because adjacent symbols at the output of the encoder are separated in time by the interleaving process there is a time delay. The time delay is a function of the interleaving depth. If the time delay is reduced by reducing the interleaving depth, the time duration of a signal fade which the system can tolerate by correcting the errors which occur as a result of the fade, is also reduced. For example, with an interleaving depth of 256 the system can tolerate a signal fade of up to 5.12 seconds but with an interleaving depth of 128 the system can tolerate a signal fade of up to 2.56 seconds.

The second problem associated with the error-correction code is in the timing in the decoder. Although the system can tolerate fades in signal strength the system must maintain an adequate timing at the receiving end of the system. Even though errors are generated as a result of the signal fade, the ordinal location of the symbols must be maintained. If a symbol is added or deleted because of inaccurate timing at the receiving end of the system a large number of errors

will result. Therefore, the accuracy of the timing at the receiving end of the system must be maintained even during signal fading conditions. The timing at the receiving end of the system may also be called the clock or bit-timing.

One technique that is often used to derive bit-timing at the receiving end of the system with modulation schemes similar to the modulation scheme used in the Fade-Resistant Modem is the phase-lock loop. With the phase-lock loop the phase relationship between the detected output of the demodulator and a local signal generator are compared. The output of the comparator (phase detector) is used to derive a clock which is in phase with the digital output of the demodulator (Reference 13). Due to the structure of the signal fading which occurs as a result of ionospheric scintillation, and primarily the duration of the signal fades, the phase-lock loop is not necessarily the ideal technique for deriving bit-timing under these conditions.

One approach for deriving bit-timing from a binary sequence where fading due to ionospheric scintillation is a problem would be to extract timing when there is a sufficiently strong signal and make no changes in the timing during fades. Digital systems are normally designed so that transitions in the binary sequence occur at multiples of a fixed time interval. Transitions in the binary sequence other than at these fixed time intervals are generally due to disturbances in the transmission channel. These disturbances may be the result of a number of factors including signal fading and/or interference.

By analyzing the time relationships of transitions in the binary sequence, switching of the binary sequence which occurred due to fading in the channel (invalid data) can be distinguished from the proper binary sequence which resulted from a sufficiently strong signal (valid data). Bit-timing could then be derived during a valid data time interval and updated only during valid data time intervals which follow. A problem with this technique is in the stability of the clock selected for use as the system clock. This clock must remain stable during the invalid data interval.

One technique which could be used to derive a stable clock for use in the receiving end of the system would be to derive the clock directly from a stable frequency source (the standard) so that the derived clock would have essentially the same stability as the standard. If eight distinct clocks were derived from the standard, with all clocks of the same frequency but displaced in phase by a difference of 45 degrees from adjacent clocks, at least one of these clocks could be used as the clock for processing. Since the phase relationship between the binary sequence and the clock is normally not required to be perfect, the selected clock, the "Best Fit" clock, should be sufficient for use in the deinterleaver-decoder at the receiving end of the system.

# SECTION III

# BIT-TIMING EXTRACTOR

## GENERAL

This section contains a description of a Bit-Timing Extractor which operates by differentiating between valid data and invalid data, and selects a "Best Fit" clock from among eight discrete clocks of the same frequency but displaced in phase by 45 degrees. The stability of each of the eight clocks is sufficient for use in a 150 b/s digital communications system which operates with signal fade durations of up to five seconds. This Bit-Timing Extractor was designed, built and tested in the laboratory as a part of the Fade-Resistant Modem described previously.

## REVIEW OF LITERATURE

The extraction of bit-timing from a binary sequence is often one of the problems associated with the design of a digital communications system. Quite often the return-to-zero (RZ) technique is used to facilitate bit-timing extraction. With the RZ technique the binary sequence switches to a neutral state between bits and bit-timing is extracted from this repetitive sequence. On the other hand, the non-return-to-zero (NRZ) (Reference 14) technique is often selected for use in digital communications systems because the NRZ technique is normally more efficient in terms of bandwidth and signal-to-noise (S/N) requirements than the comparable RZ technique.

For digital communications systems which operate at an expected low BER and utilize the RZ technique bit-timing is often derived from the repetitive transitions in the sequence. For the more efficient RZ technique the phase-lock loop is often used to extract bit-timing (References 13 and 15). Since the phase-lock loop does not normally distinguish between a noisy signal and a usable signal it will also try to track on noise. With signal fades of up to five seconds this could be a problem. In addition, even under strong signal conditions a mark hold (or space hold) sequence (no transitions) could be a problem for the phase-lock loop technique.

An ideal bit-timing extraction technique for use in a system which is required to operate through long duration signal fades and mark hold (or space hold) sequences, as well as the normal usable toggling binary sequence, would derive bit-timing during the usable binary sequence and have sufficient stability to maintain adequate bit-timing during the signal fades and mark hold (or space hold) sequences. The Bit-Timing Extractor described herein was conceived to meet these requirements.

## GENERAL DESCRIPTION

The Bit-Timing Extractor can be divided into eight basic sections. Figure 4 is a block diagram of the Bit-Timing Extractor which shows the interconnections of these eight sections.

A very stable clock oscillator is contained in the Clock Generator Circuit. From this stable frequency source eight separate clocks are derived, all of the same frequency but displaced in phase from adjacent

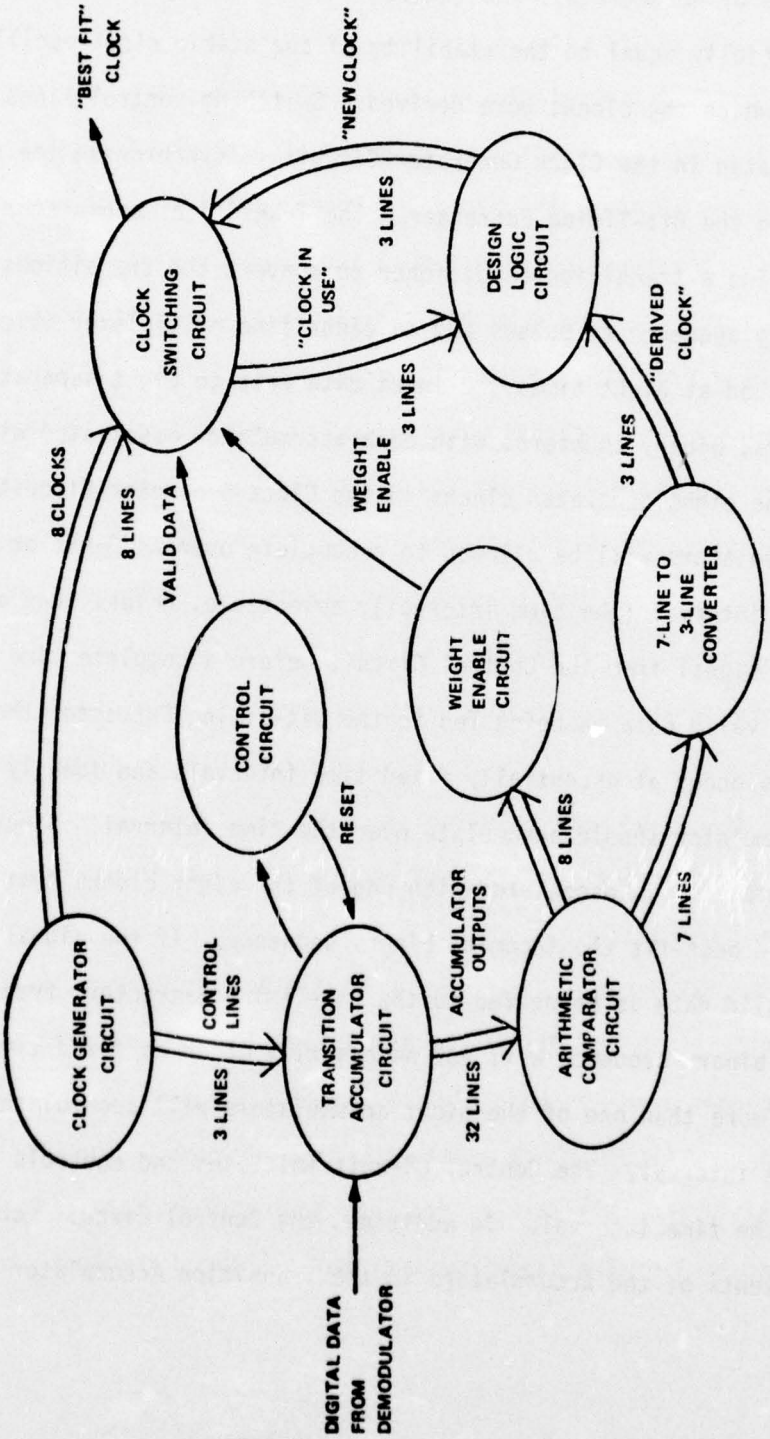



Figure 4. Block Diagram of the Bit-Timing Extractor

clocks by 45 degrees. The frequency stability of each clock is essentially equal to the stability of the stable clock oscillator from which the clocks were derived. Switching control lines are also generated in the Clock Generator Circuit to synchronize the switching within the Bit-Timing Extractor. The Transition Accumulator Circuit contains a transition conditioner to convert the transitions in the binary sequence to pulses and an eight line multiplexer which is switched at eight times the input data rate to eight separate accumulators, binary counters, with each accumulator associated with one of the eight generated clocks in the Clock Generator Circuit. The accumulators will be allowed to accumulate over an 8-bit or 16-bit time interval (the time interval), selectable, unless they are cleared by a signal from the Control Circuit before a complete time interval. When valid data is being fed to the Bit-Timing Extractor the transitions occur at essentially fixed time intervals and ideally only one accumulator should accumulate over the time interval. Since this accumulator is associated with one of the eight clocks that clock would best-fit the incoming binary sequence. If the signal fades and invalid data is being fed to the Bit-Timing Extractor, transitions in the binary sequence will not necessarily occur at fixed time intervals and more than one of the eight accumulators will accumulate during the time interval. The Control Circuit initiates and controls the length of the time interval. In addition, the Control Circuit monitors the contents of the accumulators in the Transition Accumulator Circuit

to determine whether the binary sequence is valid or invalid. Although the best indication of valid data is when only one accumulator has accumulated, the Control Circuit can be switched such that more than one accumulator may contain transitions under valid data conditions. Once invalid data is indicated during the time interval the system will reset. If the data is valid at the end of the time interval, the contents of the eight accumulators are compared in the Digital Comparison Circuit to determine which accumulator contains the greater number of transitions. Under valid data conditions the clock associated with this accumulator is most likely the "Best-Fit" clock. The Weight Enable Circuit compares the accumulated transitions (weight) of the accumulator with greatest weight with a predetermined weight (selectable) to determine if the accumulated weight is sufficient to justify updating or if the accumulated weight is insufficient and updating should be inhibited. The 7-line output of the Digital Comparison Circuit is converted to a 3-line output in the 7-line to 3-line Converter Circuit. This 3-line output is called the Derived Clock and is compared to the clock presently in use, the Present Clock, in the Decision Logic Circuit. If the two clocks are different, the Decision Logic Circuit will generate a New Clock which will be a clock adjacent to the Present Clock and in the direction of the Derived Clock. This Clock Switching Circuit will update the Present Clock to the New Clock if the data is valid and the contents of the accumulator are sufficient to justify a change in clocks. If there is invalid data and/or the

contents are insufficient to justify a change, the Clock Switching Circuit will not update but will hold with the Present Clock.

DETAILED DESCRIPTION

This section contains a detailed description of each of the sections of the Bit-Timing Extractor and discussion of the operation of the individual sections and how these sections operate as a unit to perform the bit-timing extraction function.

The Clock Generator Circuit consists of a 9.6 kilobit (kb/s) clock oscillator and a series of dividers as shown in Figure 5. The clock oscillator is a temperature compensated crystal oscillator (TCXO) with an accuracy of $\pm$.0001%. The clock oscillator feeds a network of dividers to generate the eight clocks of exactly the same frequency (150 Hz) with each clock displaced in phase from the clocks adjacent to it by 45 degrees. One of these clocks will be selected as the clock which best fits the incoming binary sequence. We will refer to this clock as the "Best-Fit Clock." To synchronize the remaining portion of the Bit-Timing Extractor with the eight generated clocks three control lines (A, B and C) from the Clock Generator Circuit are used to synchronize the timing in the Bit-Timing Extractor.

The binary output from the data demodulator section of the Fade-Resistant Modem is fed to the Transition Accumulator Circuit in the Bit-Timing Extractor. The logic block diagram of this circuit is shown in Figure 6. This circuit converts the transitions in the binary sequence output of the data demodulator to pulses and

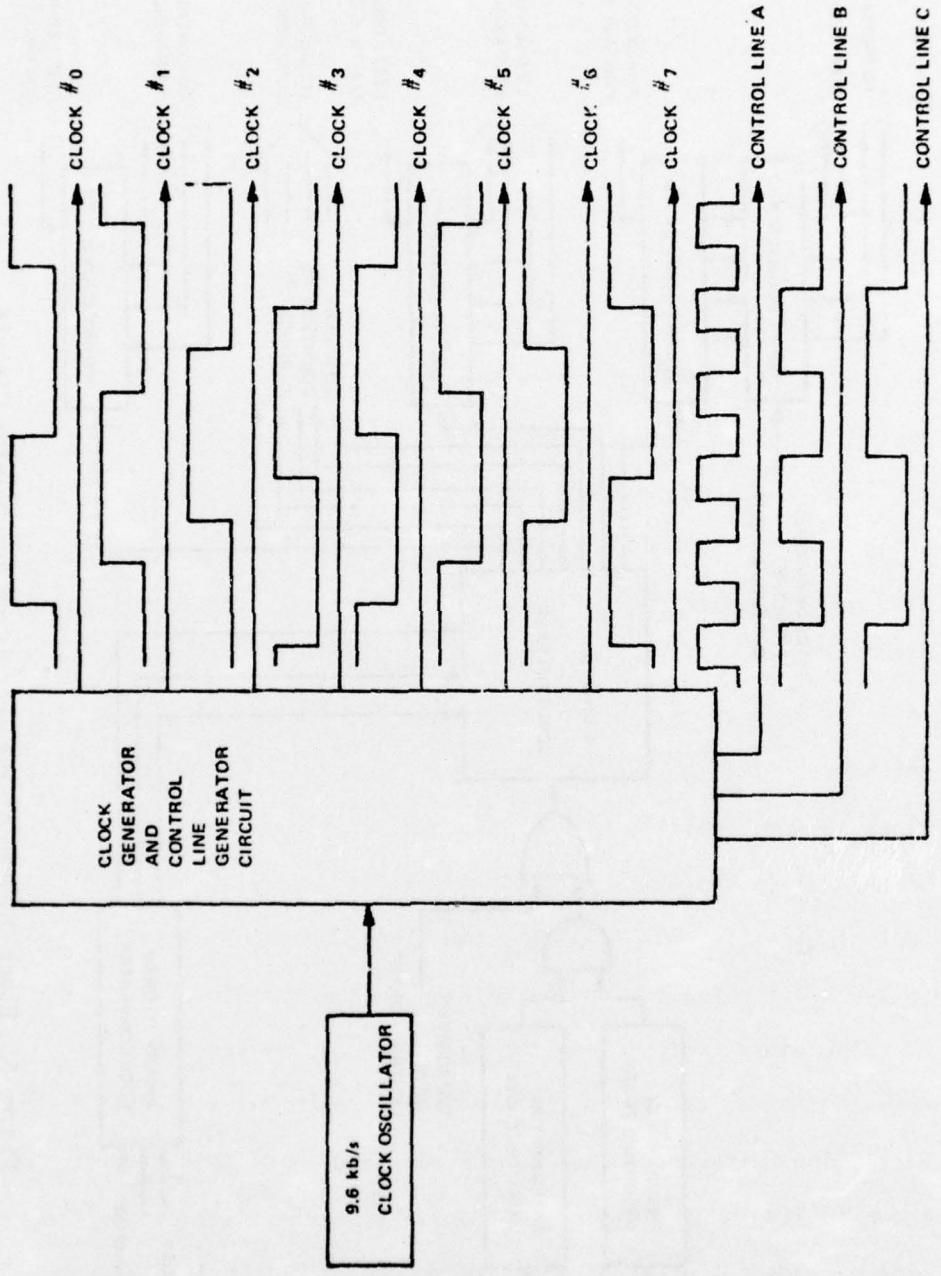



Figure 5. Block Diagram of the Clock Generator Circuit

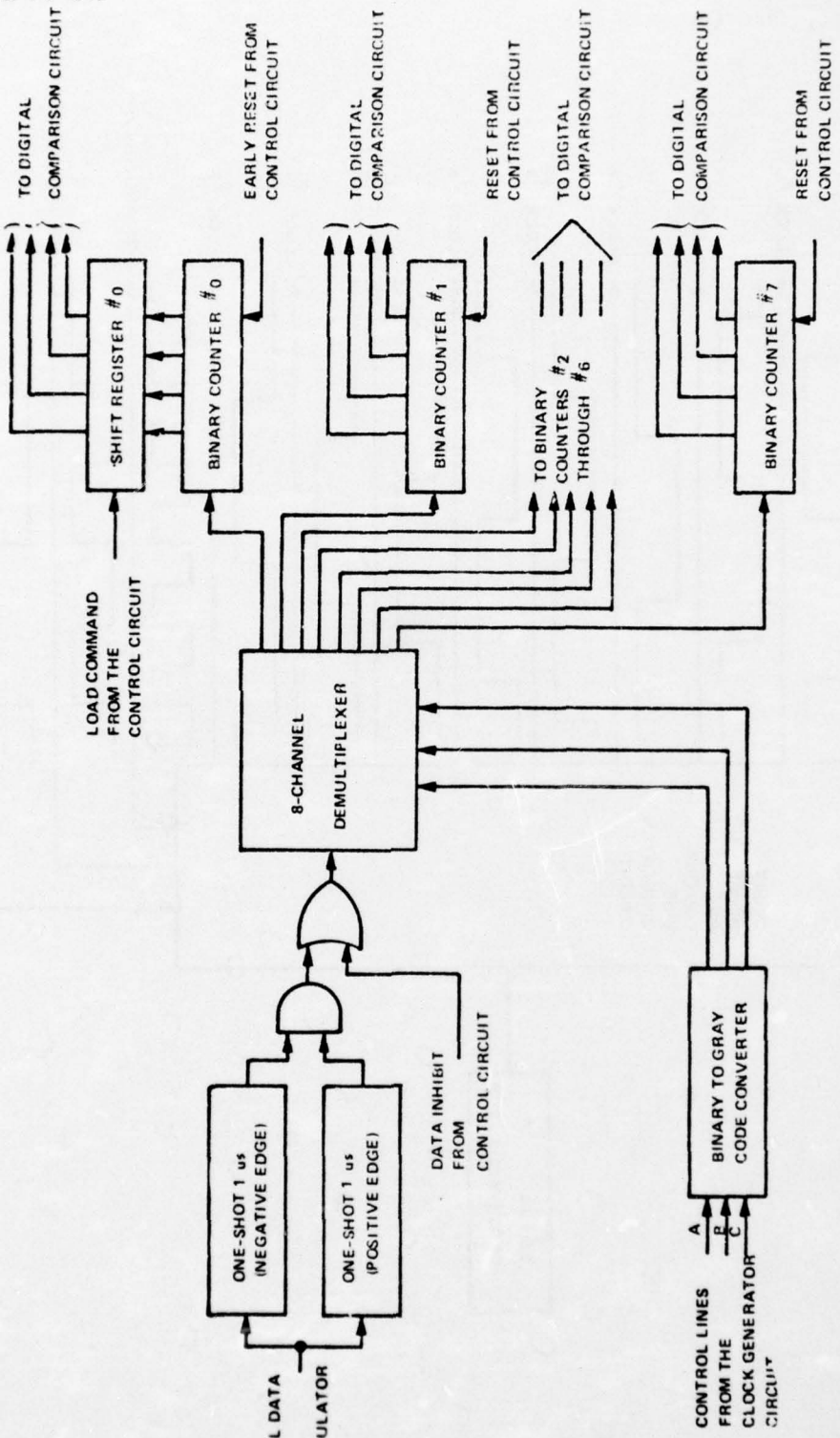



Figure 6. Block Diagram of the Transition Accumulator Circuit

demultiplexes the pulse stream to eight different accumulators, binary counters, with each accumulator associated with one of the eight clocks generated in the Clock Generator Circuit.

The switching of the Demultiplexer is controlled by the A, B and C control lines which are generated in the Clock Generator Circuit. The binary sequence of the control lines is converted to Gray Code in the Binary to Gray Code Converter. Gray Code switching of the 8-Channel Demultiplexer will prevent any indeterminate states from occurring during switching since only one line will be switched at a time.

The binary sequence from the data demodulator is fed to two one-shots each with a time constant of approximately one microsecond (μs). One one-shot triggers on negative transitions of the binary output and the other one-shot triggers on position transitions. The complementary output of each one-shot is fed to an AND gate. The AND gate output will transition to the low state when there is a transition in the binary output. The OR gate following the AND gate is used to inhibit the input to the Demultiplexer when an invalid binary sequence is detected. When an invalid binary sequence is detected the input to the 8-Channel Demultiplexer will be held in a high state until the system is set to start a new time interval.

The 8-Channel Demultiplexer is sequenced at a rate eight times the switching rate of the binary output from the data demodulator. Each of the eight sub-intervals is associated with one of the clocks generated in the Clock Generator Circuit. Each of the eight output

lines of the Demultiplexer is fed to an accumulator and a flip/flop (F/F). Each accumulator will count, or accumulate, the transitions which occur during the particular sub-interval to which it is associated.

The eight accumulators will be allowed to accumulate for either eight or sixteen sequences of the Demultiplexer. The particular time interval sequence is selectable. Eight sequences are equivalent in time to 8/150 seconds while sixteen sequences are equivalent to 16/150 seconds. During the final sequence of a time interval and following the sub-interval associated with Binary Counter #0, the contents of Binary Counter #0 are shifted to Shift-Register #0. This command to load Shift-Register #0 comes from the Control Circuit. By shifting the contents of Binary Counter #0 to a Shift-Register the contents of the eight accumulators can be compared at the start of the next time interval while Binary Counter #0 is in the accumulating mode. The contents of Shift-Register #0 and the seven higher numbered accumulators #1 through #7 are fed to the Arithmetic Comparator Circuit to determine which accumulator accumulated the most transitions during the time interval.

The Control Circuit performs a monitoring and control function within the Bit-Timing Extractor. The Control Circuit initiates the time interval and controls the length of the time interval, including early reset. Secondly, the Control Circuit monitors the eight flip/flops (F/F #0 through F/F #7) in the Transition Accumulator Circuit

to determine the number of sub-intervals which accumulated data transitions during the time interval. A third function of the Control Circuit is to inhibit updating of the output clock if no data transitions occurred during the time interval. The Control Circuit enables updating of the output clock if the data is valid during the time interval. To be valid the number of sub-interval flip/flops set in the Transition Accumulator Circuit must not exceed a predetermined setting (selectable) during the time interval and the number of transitions in the accumulator with the greatest number of accumulated transitions must be equal to or greater than a predetermined setting (selectable). The switching in the Control Circuit is synchronized with other circuits of the Bit-Timing Extractor by utilizing control line C from the Clock Generator Circuit to derive a time base in the Control Circuit. Figure 7 is a logic block diagram of the Control Circuit.

Control line C from the Clock Generator Circuit is fed to the "DEFG" Binary Counter in the Control Circuit. The outputs of this counter are used to set the time interval over which time transitions in the binary output of the data demodulator are accumulated. The sequence of events within the Control Circuit is initiated when the D, E, F and G outputs of the "DEFG" Binary Counter are in the high state and control line C transitions to the high state for a time interval equivalent to 16 bits. For a time interval equivalent to 8 bits only the D, E and F outputs need to be in a high state when

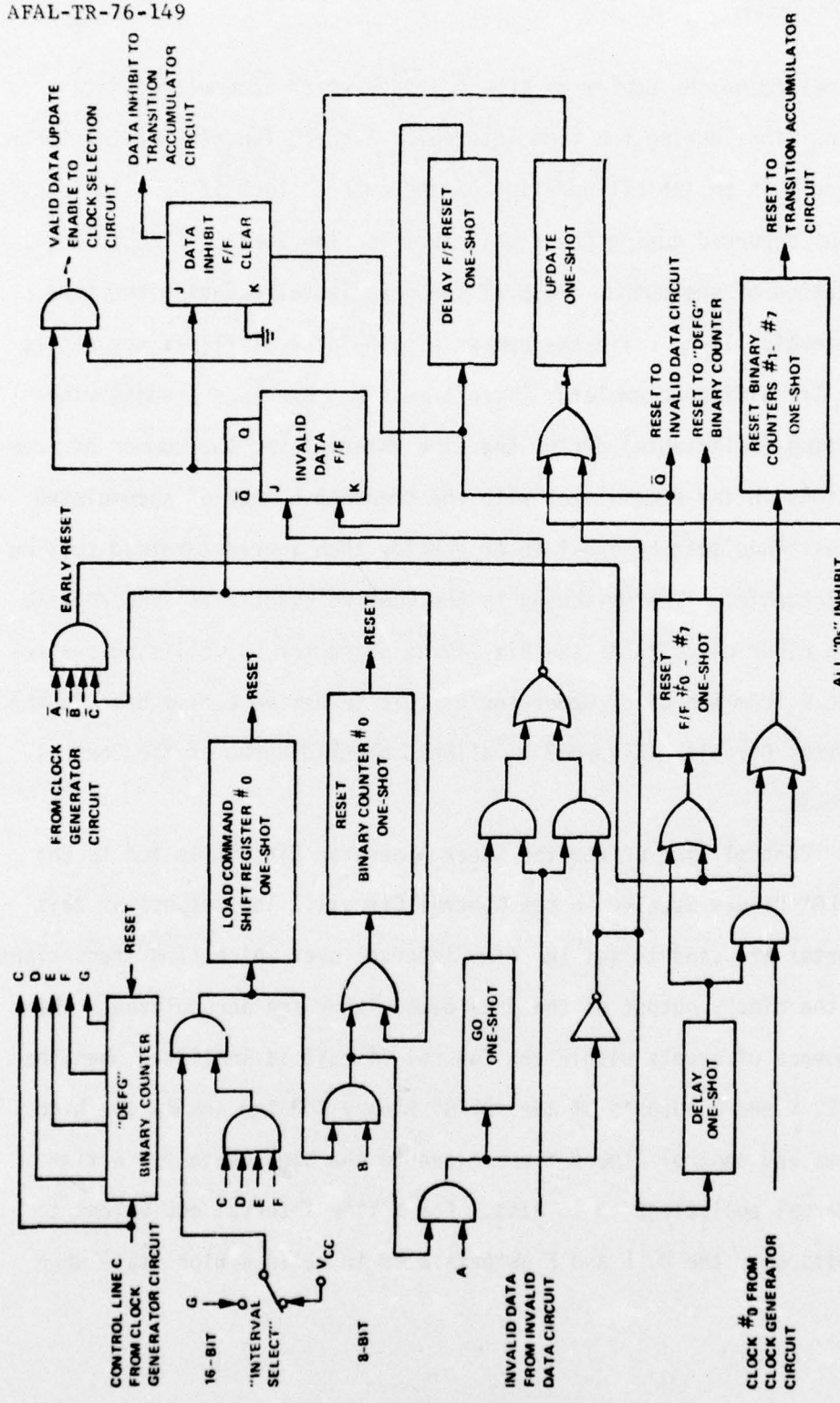



Figure 7. Block Diagram of the Control Circuit

control line C transitions to the high state. The time interval is a selectable function. When the sequence is initiated the Load Command Shift Register #0 One-Shot is triggered. The output of this one-shot loads the contents of Binary Counter #0 of the Transition Accumulator Circuit to Shift Register #0 in the Transition Accumulator Circuit. As discussed previously, this will allow Binary Counter #0 to accumulate at the start of a new time interval cycle while data accumulated during the previous time interval is being processed. Once Shift Register #0 is loaded Binary Counter #0 in the Transition Accumulator Circuit is cleared when control line B transitions to a high state and triggers the Reset Binary Counter #0 One-Shot. The output of this one-shot clears Binary Counter #0. As the sequence continues, when control line A transitions to a high state the Go One-Shot is triggered. The time constant of this one-shot is set to hold the output in the high state for approximately 95 percent of the time duration of the last sub-interval. This will allow an invalid data signal from the Invalid Data Circuit to inhibit updating the system during the time when the output of this one-shot is high with the data accumulated during this time interval. Once the Go One-Shot resets to the low state without an invalid data signal, the system is committed to an update unless the system is inhibited from updating by other inhibiting circuits.

In the event that an invalid data sequence is received during a time interval the Invalid Data F/F will be set, with the Q output

going to a high state. The complementary output of Q will be in a low state and will inhibit the possible output of an update enable pulse. In addition, the transition of the complementary output of the Invalid Data F/F to the low state will set the Data Inhibit F/F. The output of this F/F is fed to the Transition Accumulator Circuit to inhibit further accumulations of transitions until the circuit is ready to start a new time interval. This new time interval will start when the B and C control lines are all in the low state and control line A transitions to the low state.

The Q output of the Invalid Data F/F is also used to initiate an early reset of the system. When the Invalid Data F/F is switched to the high state, due to invalid data, Binary Counter #0 in the Transition Accumulator Circuit is reset and the Transition Accumulator Circuit is inhibited until the circuit is ready to start a new time interval. At the start of the time interval Binary Counters #1 through #7 are reset, F/Fs #0 through #7 are reset and the "DEFG" Binary Counter is reset. This removes the invalid data signal and the Data Inhibit F/F is reset, thus allowing the Transition Accumulator Circuit to accumulate data. The Invalid Data F/F is then reset following a slight delay. This delay insures that the system is ready with no invalid data signal before the Invalid Data F/F is reset. When the Invalid Data F/F is reset the invalid data sequence is complete and the system is into a new time interval.

Once a time interval is complete, and there was no invalid data signal, the Update One-Shot will be triggered unless there were no transitions in the binary output during the time interval. If there were no transitions in the binary output during the time interval the input to the Update One-Shot will be inhibited and there will be no valid data update enable to the Clock Selection Circuit. Following a slight delay F/Fs #0 through #7 are reset and the "DEFG" Binary Counter is reset. When Clock #0 transitions to the high state Binary Counters #1 through #7 are reset and the system is now into a new time interval. Although data is being processed and the system is being reset following the triggering of the Update One-Shot and the Delay One-Shot, Binary Counter #0 is being allowed to accumulate at the start of a new time interval.

The contents of the eight accumulators in the Transition Accumulator Circuit are compared two at a time in the Arithmetic Comparator Circuit to determine which of the eight accumulators accumulated the most transitions during the time interval. Figure 8 is a logic block diagram of the Arithmetic Comparator Circuit.

Initially, Binary Counters #0 and #1 are compared, #2 and #3 are compared, #4 and #5 are compared, and #6 and #7 are compared. From these four comparisons the contents of the binary counter with the greater number of transitions are gated on for further digital comparison. This process of digital comparison is repeated one more time with a total of seven digital comparisons being necessary to

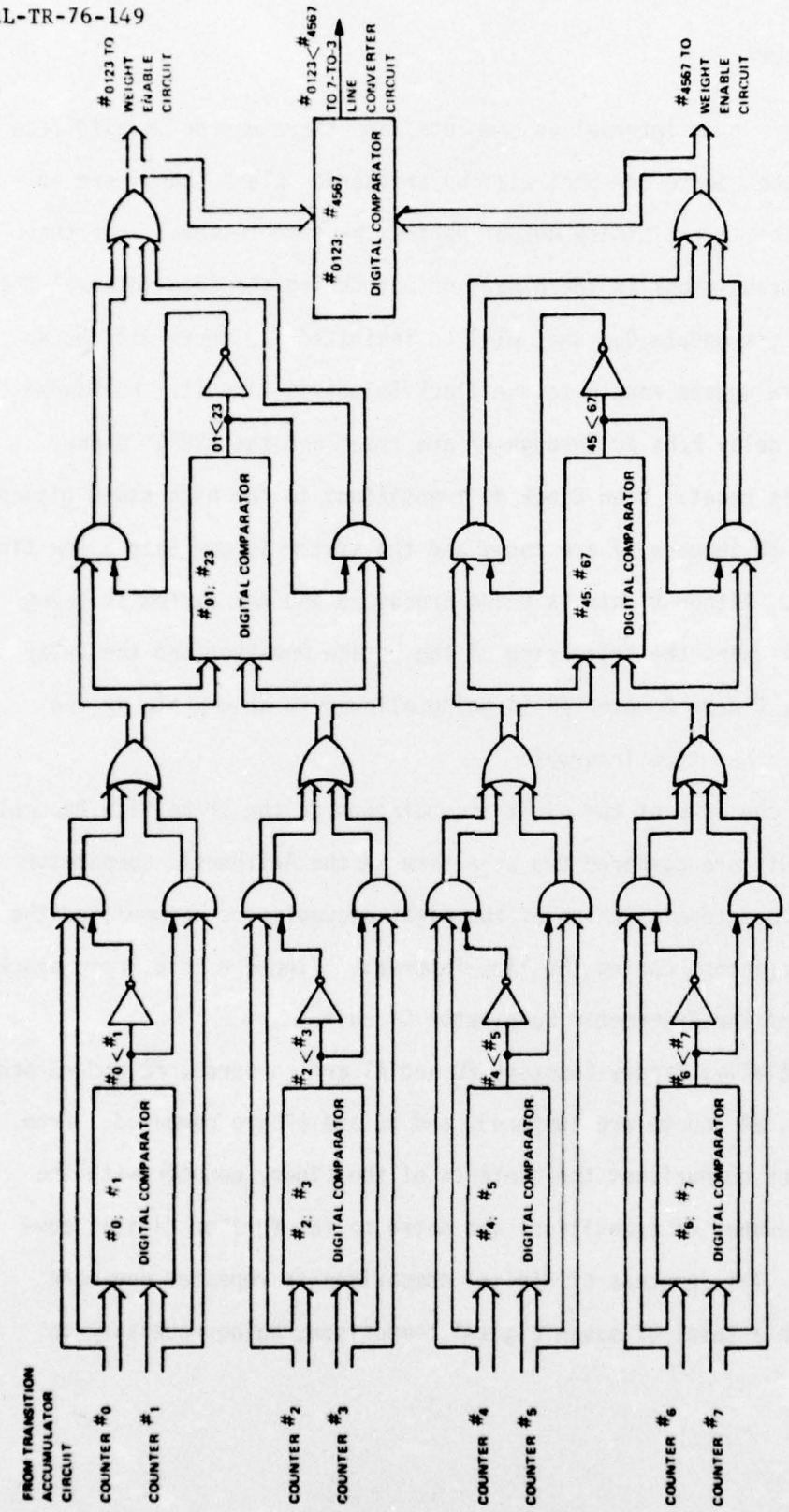



Figure 8. Block Diagram of the Arithmetic Comparator Circuit

determine which of the seven accumulators had the greatest number of transitions. If the contents of two accumulators being compared are equal, then the lower numbered counter is arbitrarily selected.

Figure 9 is a logic block diagram of the Weight Enable Circuit. This circuit continues the digital comparison process started in the Arithmetic Comparator Circuit until the contents of the accumulator with the greatest number of transitions is selected for comparison with a predetermined weight (selectable). When the contents of the accumulator with the greatest number of transitions is equal to or greater than the predetermined weight the output will enable the Clock Selection Circuit if there is an update enable from the Control Circuit.

The digital outputs of the seven digital comparators are fed to the 7-line to 3-line Converter Circuit. This circuit converts the seven information bits from the Digital Comparison Circuit to three bits which, in turn, can be used to identify one of the eight clocks. Figure 10 is a logic block diagram of the 7-line to 3-line Converter Circuit. This figure also contains a table which associates the inputs and outputs of the 7-line to 3-line Converter Circuit with specific clocks.

The output of the 7-line to 3-line Converter Circuit is termed the "Derived Clock" since this is the clock that was, in fact, derived from the binary output. The "Derived Clock" is fed to the Digital Logic Circuit. Figure 11 is a logic block diagram of the Digital

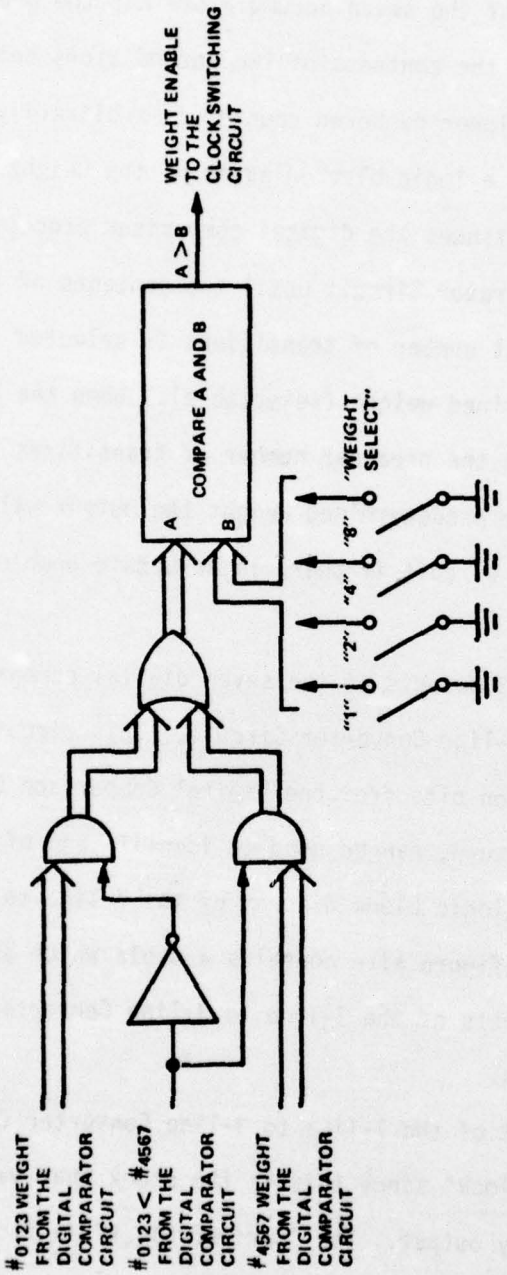
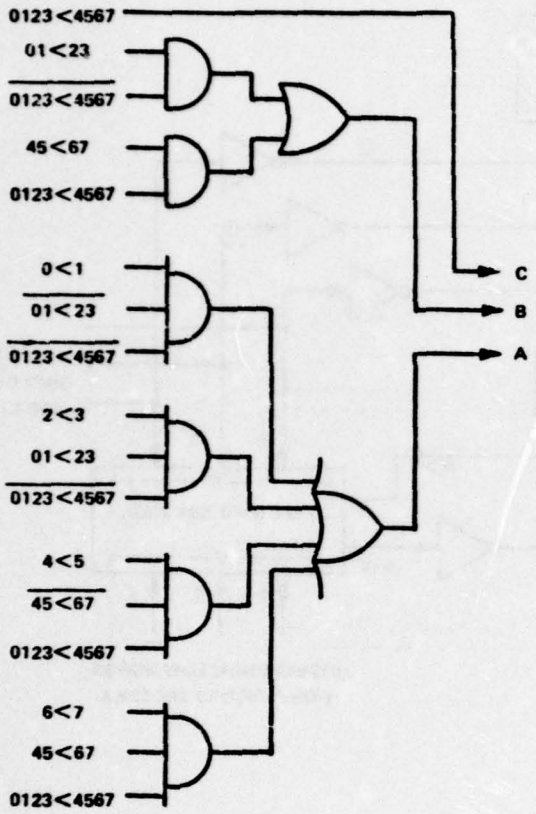



Figure 9. Block Diagram of the Weight Enable Circuit




| INPUTS | | | | | | | OUTPUTS | | | CLOCK |
|---|---|---|---|---|---|---|---|---|---|---|
| 0<1 | 2<3 | 4<5 | 6<7 | 01<23 | 45<67 | 0123<4567 | C | B | A | NUMBER |
| 0 | - | - | - | 0 | - | 0 | 0 | 0 | 0 | 0 |
| 1 | - | - | - | 0 | - | 0 | 0 | 0 | 1 | 1 |
| - | 0 | - | - | 1 | - | 0 | 0 | 1 | 0 | 2 |
| - | 1 | - | - | 1 | - | 0 | 0 | 1 | 1 | 3 |
| - | - | 0 | - | - | 0 | 1 | 1 | 0 | 0 | 4 |
| - | - | 1 | - | - | 0 | 1 | 1 | 0 | 1 | 5 |
| - | - | - | 0 | - | 1 | 1 | 1 | 1 | 0 | 6 |
| - | - | - | 1 | - | 1 | 1 | 1 | 1 | 1 | 7 |

Figure 10. Block Diagram of the 7-Line to 3-Line Converter Circuit

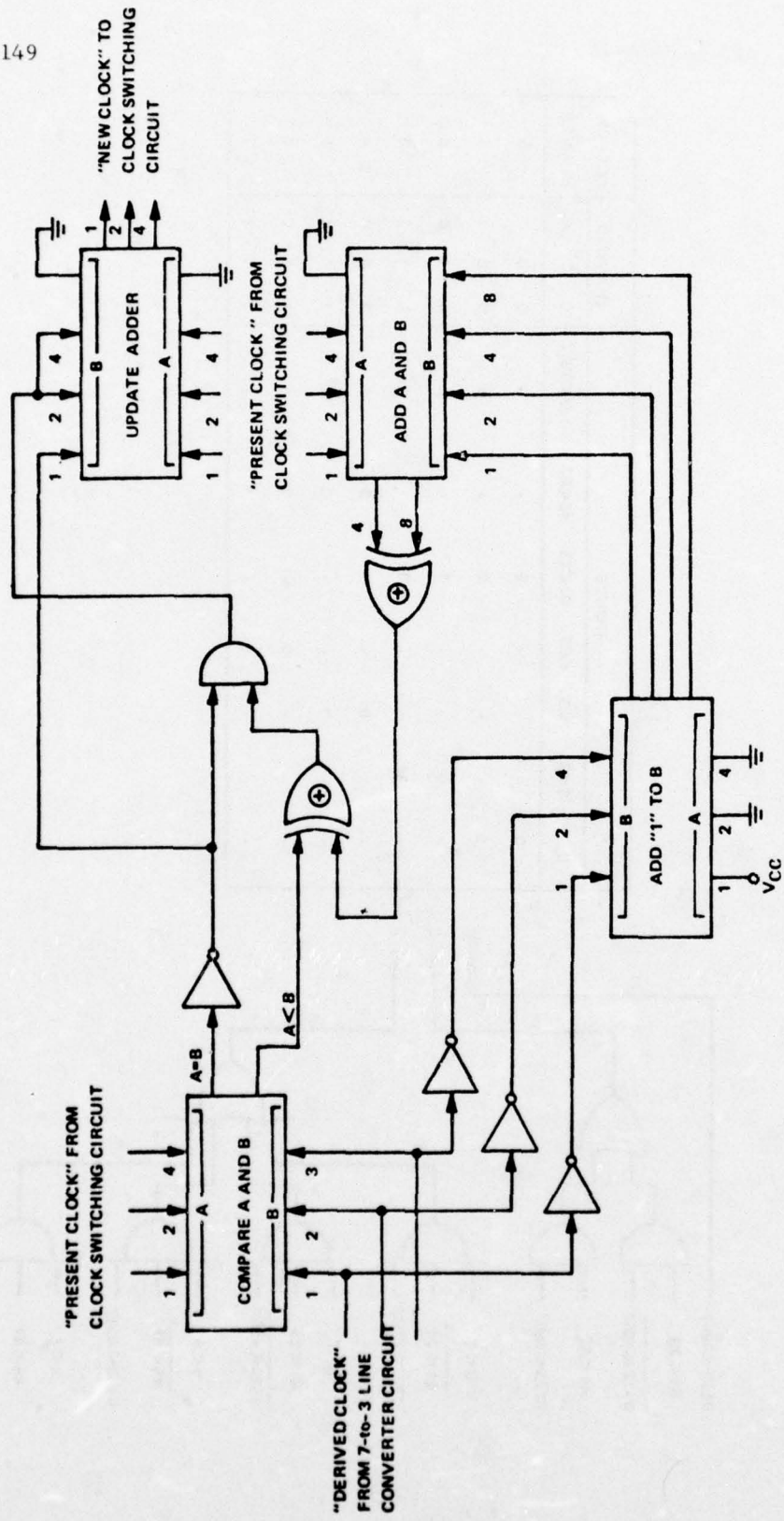



Figure 11. Block Diagram of the Digital Logic Circuit

Logic Circuit. This circuit compares the clock which is presently being used in the system, the "Present Clock," with the "Derived Clock" and generates a "New Clock." The system will switch to the "New Clock" if there is a valid data update enable pulse from the Control Circuit and if there is sufficient weight. When the "New Clock" is switched into the system it becomes the "Present Clock."

There are limitations on what "New Clock" can be generated. First of all, the "New Clock" can only be a clock adjacent to the "Present Clock" or a clock which is the same as the "Present Clock." When the "Present Clock" and the "Derived Clock" are different, the "New Clock" will be the adjacent clock to the "Present Clock" and in the shortest direction to the "Derived Clock." If the difference in the two clocks is four the "New Clock" will be derived by adding one to the "Present Clock." The "New Clock" is fed to the Clock Selection Circuit.

Figure 12 is a logic block diagram of the Clock Selection Circuit. The eight clocks, Clocks #0 through #7, are fed to this circuit and from these eight clocks one clock is switched to the output as the "Best-Fit" clock. The information stored in S-R "A" controls which clock is to be switched through the Data Select Multiplexer. The positive transition of the clock at the output of the multiplexer triggers the Cover One-Shot. The time constant of this one-shot is set for approximately 3 ms and the output of this one-shot will hold the "Best-Fit" clock in the high state while new information, the "New Clock," is switched into S-R "A". The "New Clock" which was

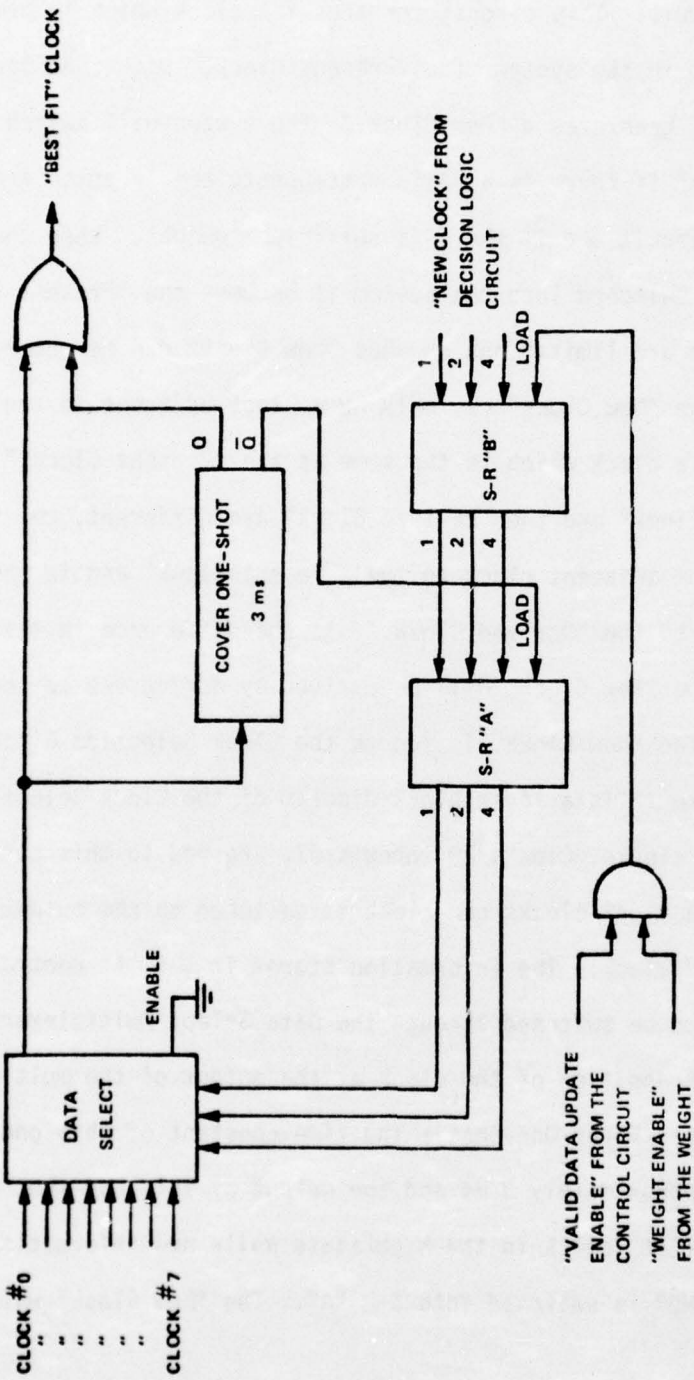



Figure 12. Block Diagram of the Clock Selection Circuit

derived is fed to a parallel-in parallel-out shift-register, S-R "B", in the Clock Selection Circuit. This "New Clock" information will only be loaded into S-R "B" if there is sufficient weight and there is a valid data update enable signal from the Control Circuit. Once the "New Clock" information is loaded into S-R "B" this "New Clock" information is fed to S-R "A" and will be loaded into S-R "A" when the "Present Clock," or "Best-Fit" clock, transitions to high state.

There are two circuits which are used in conjunction with the Control Circuit to determine whether the transitions in a time interval are valid. Figure 13 is a logic block diagram of Valid Data Circuit. This block diagram contains the 8-Channel Demultiplexer of the Transition Accumulator Circuit. The outputs of this 8-Channel Demultiplexer are fed to the eight accumulators and also to eight flip/flop, OR gate combinations as shown in the figure. The output of each of the eight flip/flops feeds an 8-Channel Multiplexer which is switched with the 8-Channel Demultiplexer. The output of the 8-Channel Multiplexer feeds a Binary Counter and the contents of this counter are compared in a comparator with a predetermined invalid data weight setting (selectable). When the contents of the Binary Counter exceeds the setting of the invalid data weight setting there is an output to the Control Circuit indicating invalid data. The outputs of the eight flip/flops are normally low and will be set high if a transition occurs during that particular sub-interval. This will trigger the Binary Counter for one count and that OR gate will be inhibited for

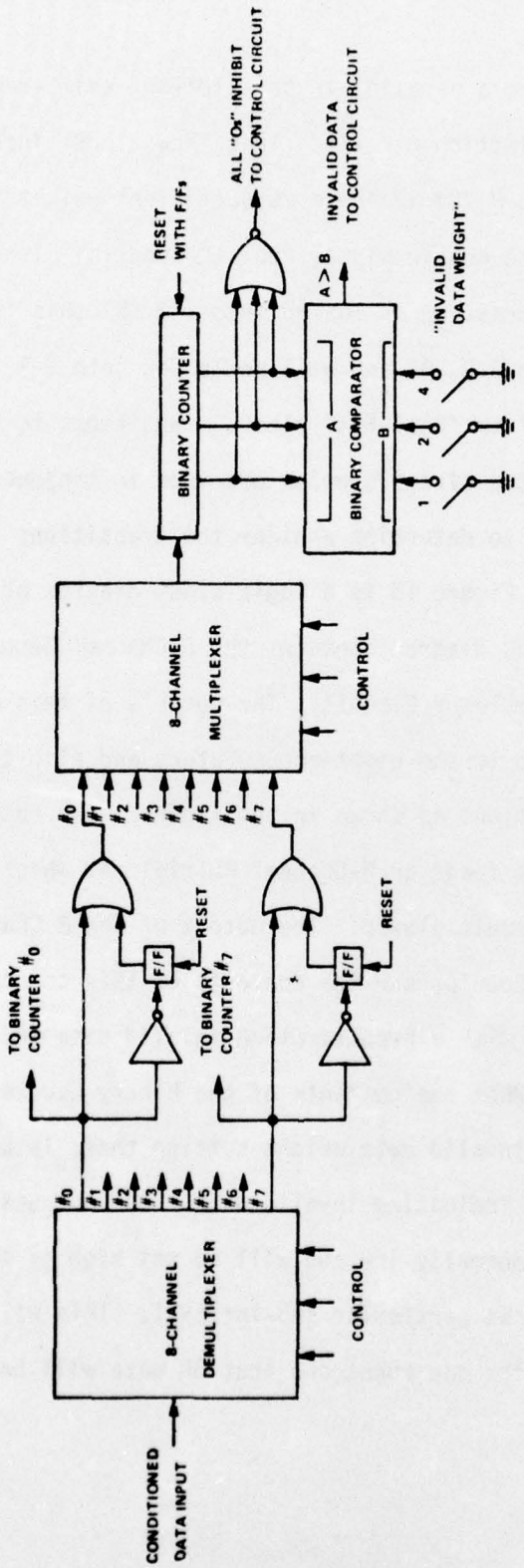



Figure 13. Block Diagram of the Valid Data Circuit

the remainder of the time interval. Thus the Binary Counter will only count the number of sub-intervals containing transitions during a time interval. The Binary Counter and the eight flip/flops are reset by the Control Circuit either at the end of a time interval or by an early reset command.

The outputs of the Binary Counter are also monitored to determine if there were no transitions during the time interval. If there were no transitions during a time interval updating is inhibited. Otherwise, Clock #0 would be selected as the "Derived Clock" when no clock should be selected.

Due to the variation in the expected time between transitions in the binary output of the data demodulator as discussed previously, a special circuit was designed to compensate for this type of variation. Since the variation is in a range about the expected transition, transitions tend to occur in adjacent sub-intervals. Under these conditions transitions which occur in adjacent sub-intervals would still be valid data. The Adjacency Circuit shown in Figure 14 is designed to monitor for transitions in either two or three (selectable) adjacent channels. In the adjacency mode with an invalid data weight of two, transitions may occur in two sub-intervals but the sub-intervals must be adjacent. Otherwise, the data would be invalid. In the adjacency mode with an invalid data weight of three, transitions may occur in three sub-intervals but the sub-intervals must be adjacent or the data would be invalid. Above invalid data weights of three,

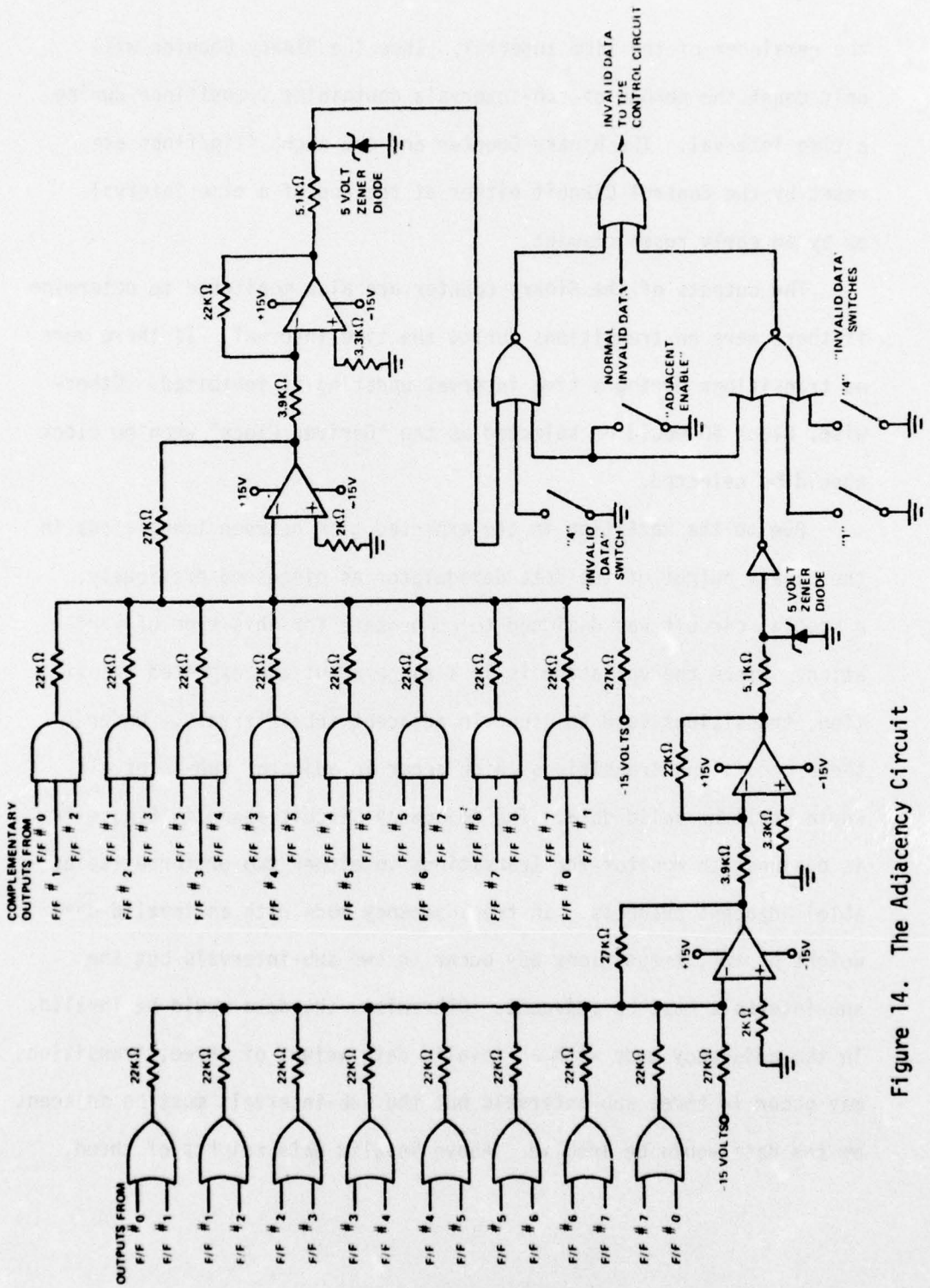



Figure 14. The Adjacency Circuit

invalid data is determined in the normal method, as opposed to the adjacency method. The adjacency requirement is selectable and the Bit-Timing Extractor can be operated in the normal method for any invalid data weight setting.

# SECTION IV

# BIT-TIMING EXTRACTOR

# ACQUISITION AND TRACKING

There are a number of performance parameters which could be used to evaluate the performance of a device which performs the function of bit-timing extraction in a digital system. The importance of each performance parameter varies with the specific system in which it is to be used. In a UHF satellite communications system which utilizes a Fade-Resistant Modem or similar type of system, acquisition time and tracking are two of the more important performance parameters of the Bit-Timing Extractor. Acquisition time can be thought of as a measure of the time required for the Bit-Timing Extractor to attain a level of operation which is sufficient to achieve adequate system performance, while tracking is the measure of the ability of the Bit-Timing Extractor to perform following acquisition.

When a valid binary sequence is initially received at the input of the Bit-Timing Extractor there could be a time delay of up to four time intervals before the clock output of the Bit-Timing Extractor is actually the clock which best fits the incoming data. If the time interval is equal to 8 bits, the time delay is approximately 213 milliseconds (ms). For a time interval equal to 16 bits this time delay is approximately 417 ms. Although the time delay could be up to four time intervals before the Bit-Timing Extractor output is the

"Best-Fit" clock, the system can achieve an adequate level of performance with the clocks adjacent to the "Best-Fit" clock. Therefore only a maximum of three time intervals is required before data can be processed. The time delay for a time interval equal to 8 bits would be 160 ms and 320 ms for an equivalent 16 bit time interval. An alternative to the possible time delay associated with initial acquisition would be to let the system select the "Best-Fit" clock from the first valid time interval as opposed to shifting one clock per time interval. Then updating would be limited to adjacent clocks.

Although the time delay associated with selecting a "Best-Fit" clock is not necessarily excessive, some of the initial data associated with selecting the "Best-Fit" clock may be lost. This lost data may be recovered by sampling the output of the data demodulator at eight times the switching rate and storing this sampled data. Then once a "Best-Fit" clock is selected the sampled data could be framed by the clock, eight sample bits to a frame, and the binary state that most likely occurred during that frame could be selected by a majority logic gate. If five or more of the samples in the frame were high the output of the majority logic gate would be high. If five or more of the samples were low the output of the majority logic gate would be low. If the sampled data were evenly divided, four high and four low, the output of the majority logic gate could be arbitrarily selected as high or low.

Once acquisition is achieved within the Bit-Timing Extractor there are a number of factors associated with the data demodulator output of

the Fade-Resistant Modem which test the ability of the Bit-Timing Extractor to track. First of all, when the signal level in the receiver drops below threshold due to a signal fade the digital output of the data demodulator is a result of noise and the Bit-Timing Extractor should not update to insure proper tracking when the signal returns following the fade. As discussed previously the Bit-Timing Extractor distinguishes valid data from invalid data by analyzing the time between transitions in the binary sequence.

A second problem associated with tracking is the variation in time between the various transitions in the binary sequence even when the quality of the data is acceptable. These variations in the time between the various transitions are a result of the technique used to detect the data in the data demodulator section of the Fade-Resistant Modem and the effects of additive noise at the lower signal-to-noise ratios. Within the data demodulator the data detection technique is essentially a three-stage process. As shown in Figure 3, following the signal spectrum conversion to 10.7 MHz the output is split, with one output fed to the mark channel and the other output to the space channel. Each of the two channels contains a 2 kHz bandpass filter, with the center frequencies of the two filters separated by 2500 Hz. The outputs of each of the two filters are amplified and then amplitude detected. Since the bandpass of each of the two filters is 2 kHz but the digital data rate is only 150 b/s, the outputs of the amplitude detectors are fed to integrators. Due to the response of the integrators

the time between transitions in the binary sequence at the output of the comparator does not occur at multiples of 1/150 seconds even under strong signal conditions at the input to the Fade-Resistant Modem with a binary sequence other than an alternating mark/space sequence. If consecutive marks, or consecutive spaces, are received there is some additional time lag when the binary sequence transitions to the other state. This phenomena tends to cause the time between transitions to occur at other than exact multiples at the output of the data demodulator. In addition, noise due to a decrease in the received signal-to-noise ratio also causes the time between binary transitions to vary.

Due to the compound effect of the data detection technique in the data demodulator and signal plus noise in the signal channel, the Bit-Timing Extractor quite often sees transitions in more than one sub-interval during any given time interval.

The Bit-Timing Extractor can compensate for the variations in time between data transitions by allowing the system to update when more than one sub-interval contains transitions during any given time interval. In addition, the binary transitions tend to occur in adjacent sub-intervals under acceptable signal-to-noise conditions. The Adjacency Circuit in the Bit-Timing Extractor can be used to detect this type of phenomena.

The format of the binary sequence also affects the performance of the Bit-Timing Extractor. The Bit-Timing Extractor performance relies on transitions in the binary sequence but in an operational system the

number of transitions vary according to a variety of factors, ranging from the type of message being sent to the technique used to send the message.

# SECTION V

# LABORATORY TESTS

## GENERAL

A series of tests was performed in the laboratory to evaluate the performance of the Bit-Timing Extractor operating as a part of the Fade-Resistant Modem. The basic test involved the BER performance of the modem under a variety of operating conditions. The tests were designed to evaluate the performance of the Bit-Timing Extractor and not necessarily to evaluate other sections of the Fade-Resistant Modem although the performance of the Fade-Resistant Modem was of interest.

## SATELLITE TESTS

The initial laboratory test was a test designed to evaluate the performance of the Bit-Timing Extractor operating as a part of a UHF satellite communication system operating under various simulated fading conditions. The basic configuration of equipment for this test is shown in Figure 15. The input/output equipment for this particular test was an Error-Checking Generator (ECG). This device generates a specific digital sequence and also analyzes the content of a binary sequence as to the error content of the sequence.

The basic test scheme involved the use of the Lincoln Experimental Satellite Number 6 (LES-6) with the UHF terminal operating full-duplex. In the full-duplex mode of operation the terminal can transmit and receive independently. In this particular case, the terminal originated

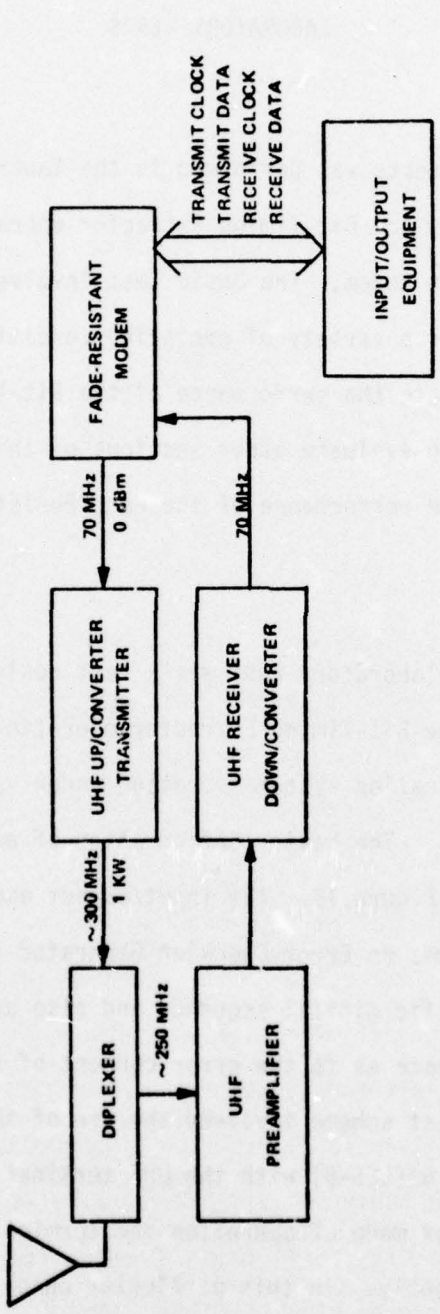



Figure 15. Equipment Configuration - Satellite Test

a UHF signal in the 300 MHz frequency range as the uplink signal to the LES-6 satellite. The satellite received the 300 MHz signal from the UHF terminal and converted the signal to the 250 MHz frequency range for retransmission as the downlink signal from the satellite. The received signal level at the input to the receiver of the UHF terminal provided a sufficiently high S/N ratio to maintain an error-free link.

This initial test was designed to evaluate the ability of the Bit-Timing Extractor to maintain adequate bit-timing when the S/N was normally high but signal outages due to simulated signal fades were induced by switching a signal attenuator in the front end of the receiver. A stop watch was used to measure the duration of the simulated signal fade. Various combinations of fades were simulated ranging from a series of short burst fades to fade durations of up to ten seconds. As long as the accumulated fade duration over approximately a 40-second interval did not exceed approximately five seconds all errors caused by the fades were corrected and the system maintained error-free performance. A four-second fade over 40 seconds would cause an uncorrected BER of approximately 5%. When the cumulative total fade duration exceeded five seconds over the 40-second time interval the errors that resulted were due to the inability of the error-correction to correct the higher BER. This initial test demonstrated the basic capability of the Bit-Timing Extractor to provide adequate bit-timing in a UHF satellite digital communications system where there is signal fading.

Following the initial test the signal level was reduced by using attenuation between the antenna and the receiver input to a level where the error-correction technique could not correct the number of errors caused by the low S/N ratio. The attenuation was then reduced, or the signal level was increased, until the error-correction technique could correct the number of errors caused by the low S/N ratio and the system operated error-free. The system was operated continuously for fifteen minutes under these conditions with error-free performance. This test demonstrated the basic capability of the Bit-Timing Extractor to provide adequate bit-timing in a UHF satellite digital communications system where the received signal level is marginal and random errors occur but are corrected by the error-correction techniques used in the system.

DEGRADATION TESTS

Following the tests with the UHF satellite a series of degradation tests were performed in the laboratory to evaluate the performance of the Bit-Timing Extractor under various S/N ratio conditions. Figure 16 shows the basic equipment configuration for this series of tests.

In this series of tests the 70 MHz output signal of the Fade-Resistant Modem was mixed with a stable frequency source of 179.1 MHz and an RF power level of +10 dBm to attain a difference frequency of 249.1 MHz. The frequency of 249.1 MHz happens to be the downlink center frequency from the LES-6 UHF satellite. The output of the mixer was fed through a 250 MHz bandpass filter to reject the unwanted

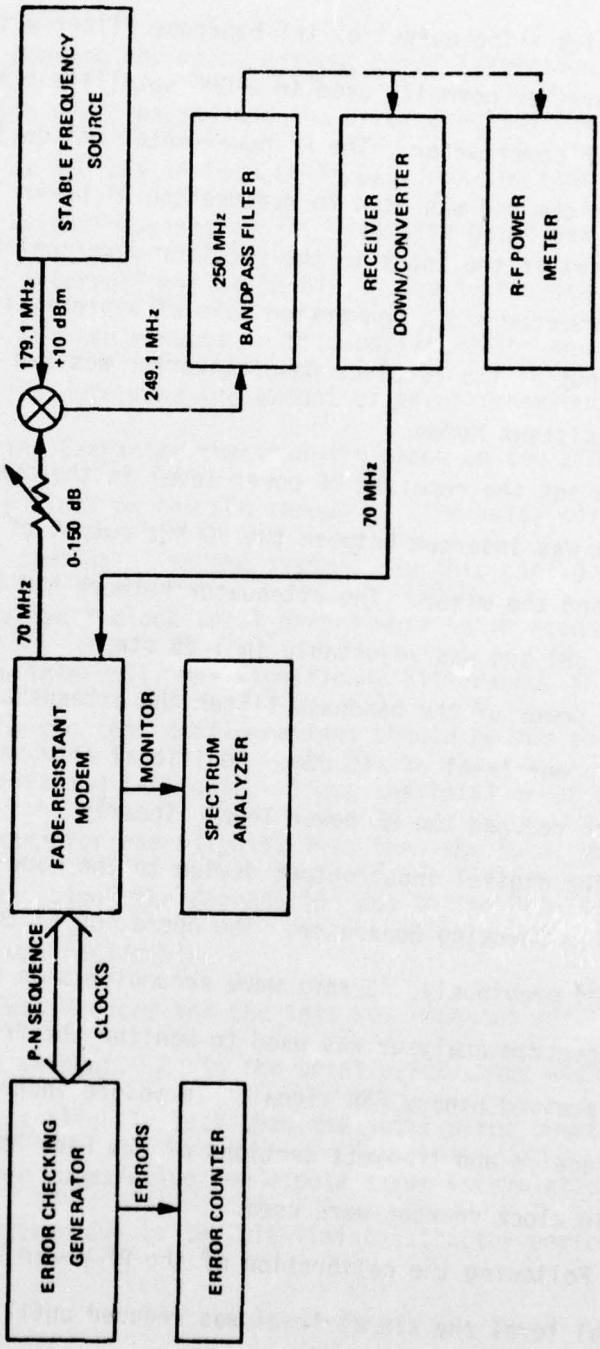



Figure 16. Equipment Configuration - Degradation Test

frequencies. The output of the bandpass filter was fed to the receiver down/converter normally used in a UHF satellite communications system or the RF power meter. The RF power meter was calibrated to read RF power in dBm and was used to measure the RF power level of the 249.1 MHz signal at the input to the receiver down/converter. The receiver down/converter had a conversion gain of approximately 25 dB. The 70 MHz output of the receiver down/converter was fed to the input to the Fade-Resistant Modem.

To set the received RF power level in the system an attenuator network was inserted between the 70 MHz output of the Fade-Resistant Modem and the mixer. The attenuator network had a range of 150 dB (0-150 dB) and was adjustable in 1 dB steps. To calibrate the RF output power of the bandpass filter the attenuator network was adjusted for a power level of -15 dBm. Additional attenuation in the attenuator network reduced the RF power level linearly.

The digital input/output device to the Fade-Resistant Modem was an Error-Checking Generator. The operation of this device was described previously. Errors were accumulated on a frequency counter. The spectrum analyzer was used to monitor the frequency spectrum about the received binary FSK signal. To insure independent operation of the receive and transmit sections of the Fade-Resistant Modem separate stable clock sources were used.

Following the calibration of the RF power level of the received signal level the signal level was reduced until the uncorrected BER

was one percent. To operate the modem without error correction the encoder-decoder section was bypassed and the Error-Checking Generator was clocked directly at 150 b/s instead of 75 b/s. On the Fade-Resistant Modem the "Weight" was set at "3," "Invalid Data" was set at "3," and the "Time Interval" was at "8-bit." The test system was operated continuously for ten minutes in this configuration and total errors were counted. To determine the extent of error contribution caused by the Bit-Timing Extractor the transmit clock on the ECG was patched to the receive clock on the ECG through a time delay circuit to compensate for the time delay in the system. In this configuration with essentially a "perfect" clock total errors were again accumulated over a ten-minute time interval. Any significant differences in total error count between the two test configurations should be due to the performance of the Bit-Timing Extractor. Since the total error count with the Bit-Timing Extractor was slightly less than the total error count with the "perfect" clock the degradation due to the Bit-Timing Extractor performance was negligible.

The signal level was reduced and the test was repeated with an uncorrected BER of ten percent. Again the total error count with the Bit-Timing Extractor was slightly less than the total error count with the "perfect" clock over comparative ten minute error accumulation time intervals. Any degradation due to the Bit-Timing Extractor performance was negligible.

A second series of degradation tests was designed to authenticate the results of the degradation tests described above. For this second series of tests the equipment configuration was similar to that shown in Figure 16. In the initial test the received signal level was reduced until the BER was one percent in the normal configuration. Once the one percent BER received power level was established the transmit data sequence was patched directly to the receive input of the ECG to insure an error-free binary sequence. Bit-timing for the receive binary sequence was derived from the binary sequence with a one percent BER. A fixed time delay was inserted between the bit-timing output of the Bit-Timing Extractor to compensate for the time delay in the demodulator section of the modem. This insured that the bit-timing output of the Bit-Timing Extractor was in phase with the data sequence although the clock was delayed. No errors were accumulated over a ten-minute time interval with the equipment in this configuration. The results of these tests agreed with the results of the first series of degradation tests with a one percent BER. The signal level was reduced and the test was repeated with an uncorrected BER of ten percent. Again no errors occurred during a ten-minute time interval. These results also tended to agree with the results of the first series of degradation tests with a ten percent BER.

To determine the signal level at which the Bit-Timing Extractor caused degradation additional attenuation was inserted to reduce the receive signal level with the transmit data sequence patched directly

to the receive input of the ECG and the receive bit-timing derived from the Bit-Timing Extractor as described in the previous test. The signal level was reduced in 1 dB steps until errors occurred due to the inability of the Bit-Timing Extractor to derive an adequate clock. Each signal level setting was monitored for approximately two minutes for the occurrence of errors. No errors occurred until the signal level was reduced 4 dB below the signal level required for a ten percent BER.

UPDATE TESTS

In the second series of degradation tests the update rate of the Bit-Timing Extractor was also measured for the different received signal levels. As discussed previously an update occurs in the Bit-Timing Extractor at the end of an 8-bit (or 16-bit) time interval if the data was valid during the interval and the weight was sufficient. Figure 17 is a plot of the number of updates per minute for various bit-error-rates. For a one percent BER an average of 67 updates occurred per minute. For a ten percent BER an average of 29 updates occurred per minute. Three dB below the ten percent BER level only 18 updates occurred per minute. This low update rate, approximately one every three seconds, at a received power level 3 dB below the ten percent signal level illustrates the ability of the Bit-Timing Extractor to track detected data from a marginal received signal level with a minimum amount of updating.

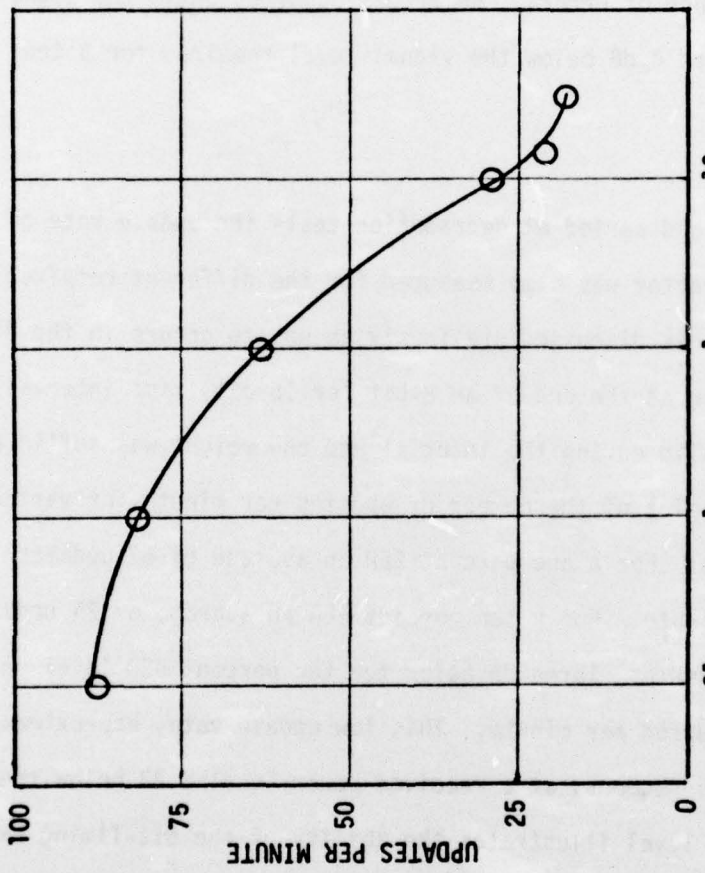



Figure 17. Updates versus BER

An uncorrected BER of ten percent would normally be unacceptable for most digital communications systems. Although the feedback decoder utilized in the Fade-Resistant Modem has the power to correct up to three errors in any twenty-two consecutive symbols the ten percent BER would not necessarily distribute the errors in this manner. Since the Bit-Timing Extractor can track below the signal levels required for a ten percent BER the analyzed results of the degradation tests indicate the feasibility of operating the Bit-Timing Extractor as a part of a modem similar to the Fade-Resistant Modem in a digital communications system operating at low signal-to-noise ratios.

MISCELLANEOUS TESTS

The binary FSK modulator/demodulator section of the Fade-Resistant Modem can be operated at 75 b/s with a minimum of modification to the circuitry designed for 150 b/s operation. The FSK modulator can be switched at either 150 b/s or 75 b/s with no change in circuitry. Only the time constant of each of the integrators in the post-detection FSK demodulator needs to be changed to optimize performance for 75 b/s operation although the degradation with no circuit modifications is only about 1 dB. Direct operation of the Fade-Resistant Modem at 75 b/s with no error correction capability would be a desirable feature since this would allow compatible operation with terminals which do not have error correction capability.

The Bit-Timing Extractor is designed to extract a 150 Hz clock from a 150 b/s binary sequence where there is a fixed time interval or

multiple of time intervals between transitions. Since the time interval between transitions for 75 b/s is a multiple of the time interval between transitions for 150 b/s the Bit-Timing Extractor should also be capable of extracting a 150 Hz clock from a 75 b/s binary sequence. The Bit-Timing Extractor can be converted to operate with 75 b/s data by dividing the 9.6 kb/s clock oscillator by two.

To determine how well the Bit-Timing Extractor performed in the 75 b/s mode (the alternate mode) a laboratory test was designed similar to the previously discussed degradation tests. The equipment configuration for this test was similar to the equipment configuration shown in Figure 16. The data rate used in the test was 75 b/s. The receive clock was the "Best-Fit" clock and was divided by two. No modification was made to any circuitry in the Fade-Resistant Modem for this test. Therefore the system was not optimized for 75 b/s operation. The "Weight" was set at "3," "Invalid Data" was set at "3," and the "Time Interval" was set at "8-bit."

The test procedure was a repeat of the procedures in the degradation tests for the one percent and ten percent BER levels. The results of the tests indicated that the Bit-Timing Extractor induced no degradation at either the one percent or ten percent BER levels. Since a ten percent BER is normally excessive in a digital communications link with no error correction and since the 75 b/s operation of the Fade-Resistant Modem is only an alternate mode the Bit-Timing Extractor was not rigorously tested in this mode. The tests conducted

did demonstrate the feasibility of operating the Fade-Resistant Modem with the 150 b/s Bit-Timing Extractor at a data rate of 75 b/s.

A second miscellaneous test involved the use of the Bit-Timing Extractor in a digital system transferring 150 b/s data in a hard-wired system. This test involved the use of the ECG with the transmit data line patched directly to the receive input of the ECG to insure error-free data. The transmit binary sequence was also fed to a network designed to interrupt the binary sequence. The interruptions ranged from a few milliseconds to a number of seconds. When interrupted the data line would be held in the low state. The output of the network was fed to the Bit-Timing Extractor. Separate stable frequency sources were used in the transmit and receive sections to derive bit-timing to insure independent operation.

The basic difference between this test and the tests described previously is the stability in the time intervals between data transitions. In the previous tests the time interval between transitions in the binary sequence varied even under strong signal conditions due to the implemented demodulation technique. In addition, when the received signal level was low, the noise caused a more pronounced variation in the time intervals between transitions. In this test the time variation between transitions in the binary sequence was minimal.

The interruptions ranged from a few milliseconds, similar to what may be caused by power line transients, to interrupts of up to ten minutes, similar to what may be caused by temporary power outages.

In all cases the derived clock was adequate for processing the data and the system operated error-free. This test illustrated the Bit-Timing Extractor's capability to operate as a clock deriving device, a quasi-filter for line transients, and a standby clock for short periods when no data is being received.

# SECTION VI

## SUMMARY AND CONCLUSIONS

The Bit-Timing Extractor was conceived and built to operate as a part of the Fade-Resistant Modem in a UHF satellite communications system. A number of tests were performed in the laboratory which demonstrated the feasibility of operating the Bit-Timing Extractor with the Fade-Resistant Modem under low signal-to-noise levels and also under a variety of simulated signal fading conditions, including fade durations of up to five seconds.

The use of the Bit-Timing Extractor is not necessarily limited to use as a part of the Fade-Resistant Modem. The Bit-Timing Extractor could be used to extract bit-timing in other similar types of digital communications systems.

## REFERENCES


1. Aarons, Jules. "A Survey of Scintillation Data and Its Relationship to Satellite Communications," AFCRL TR-70-0053, Air Force Cambridge Research Laboratory, Bedford, Massachusetts, 1970. 167 pp.

2. Foshee, James J. "A Fade-Resistant Modem for Use in a UHF Satellite Communications Link Disturbed by Ionospheric Scintillation Fading," USNC/URSI Annual Meeting (October, 1975), 60.

3. _____. "A Modem for Use in an Airborne UHF Satellite Communications Link Disturbed by Signal Fading," AIAA/AFWAL Mini-Symposium (25 March 1976), 28.

4. Stein, Seymour, and J. Jay Jones. Modern Communications Principles, McGraw-Hill Book Company, New York, 1967. 382 pp.

5. Master Test Plan (AFSATCOM). Air Force Satellite Communications System, Space and Missile Systems Organization, Air Force Systems Command, 1975. 153 pp.

6. Hamming, R. W. "Error Detecting and Correcting Codes," Bell Systems Technical Journal, 29 (April, 1950), 147-160.

7. Viterbi, Andrew J. "Error Bounds for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm," IEEE Transactions on Information Theory, IT-13 (January, 1967), 260-269.

8. Peterson, W. Wesley. "Encoding and Error-Correction Procedures for the Bose-Chaudhuri Codes," IRE Transactions on Information Theory, IT-6 (September, 1960), 459-470.

9. Abramson, N. M. "A Class of Systematic Codes for Non-Independent Errors," IRE Transactions on Information Theory, IT-5 (December, 1959), 150-157.

10. Gallager, R. G. "Lower Bounds on the Tails of Probability Distributions," Massachusetts Institute of Technology Research Laboratory of Electronics, QPR77 (1965), 277-291.

11. Lin, Shu and H. Lyne. "Some Results on Binary Convolutional Code Generators," IEEE Transactions on Information Theory, IT-3 (January, 1967), 134-139.

12. Linkabit Corporation. Instruction Manual Convolutional Encoder Feedback Decoder, 1975. 49 pp.

13. Stiffler, J. J. Theory of Synchronous Communications, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1971. 562 pp.

14. Magrab, Edward B., and Donald S. Blomquist. The Measurement of Time-Varying Phenomena. Wiley-Interscience, New York, New York, 1971. 347 pp.

15. Gardner, F. M. Phaselock Techniques. John Wiley and Sons, New York, New York, 1966. 176 pp.



☆ U. S. GOVERNMENT PRINTING OFFICE: 1976 — 657-630/974